CLAIMS

1. An apparatus comprising:

a first circuit to operate at a frequency that is dependent on a power supply voltage; and

a frequency control circuit coupled to a voltage regulator to supply power to the first circuit, and control the frequency of the first circuit.

2. The apparatus of claim 1, wherein the frequency control circuit controls the frequency of the first circuit by directing the voltage regulator to one of increase and decrease the power supply voltage.

3. The apparatus of claim 1, wherein the frequency control circuit includes a second circuit to sense the frequency of the first circuit.

4. The apparatus of claim 3, wherein the frequency control circuit directs the voltage regulator to decrease the power supply voltage as low as possible while still maintaining a minimum target frequency as sensed by the second circuit.

5. The apparatus of claim 1, wherein the frequency control circuit includes a second circuit to sense a temperature about the first circuit.

6. The apparatus of claim 5, wherein the frequency control circuit directs the voltage regulator to increase the power supply voltage to a maximum voltage allowed by a present temperature sensed by the second circuit.

7. The apparatus of claim 1, wherein the first circuit provides a clock signal.

8. The apparatus of claim 7, wherein the first circuit comprises a plurality of distributed oscillators that drive a clock distribution network.

9. The apparatus of claim 8, wherein the apparatus further comprises an element that is powered by the power supply voltage and that is driven by the clock signal.

10. The apparatus of claim 1, wherein the frequency control circuit comprises a device to issue a code representing a desired voltage.

11. The apparatus of claim 10, wherein the power supply voltage is provided by the voltage regulator based on the code.

12. The apparatus of claim 1, wherein the frequency control circuit comprises a device to receive a first clock signal and a second clock signal and to output at least a signal indicative of a desired power supply voltage level based on the first clock signal and the second clock signal.

13. The apparatus of claim 12, wherein the device is provided within a core of an integrated circuit.

14. The apparatus of claim 13, wherein the first clock signal comprises a system clock produced external from the core.

15. The apparatus of claim 1, further comprising a software selectable switch to select between at least a frequency maximizing mode and a power minimizing mode.

16. The apparatus of claim 1, wherein said frequency control circuit selects among a plurality of speed targets.

17. An apparatus comprising:

a clock distribution network;

at least one circuit element coupled to the clock distribution network to produce a clock signal on the clock distribution network, a frequency of the

clock signal being dependent on a power supply voltage applied to the at least one circuit element; and

a frequency control circuit coupled to the at least one circuit element to control the frequency of the clock signal.

18. The apparatus of claim 17, wherein the frequency control circuit controls the frequency of the clock signal by directing a voltage regulator to one of increase and decrease the power supply voltage.

19. The apparatus of claim 17, wherein the frequency control circuit includes a circuit to sense the frequency of the at least one circuit element.

20. The apparatus of claim 19, wherein the frequency control circuit directs the voltage regulator to decrease the power supply voltage as low as possible while still maintaining a minimum target frequency as sensed by the circuit.

21. The apparatus of claim 17, wherein the frequency control circuit includes a circuit to sense a temperature about the at least one circuit element.

22. The apparatus of claim 21, wherein the frequency control circuit directs the voltage regulator to increase the power supply voltage to a maximum voltage allowed by a present temperature sensed by the circuit.

23. The apparatus of claim 17, wherein the at least one circuit element provides a clock signal.

24. The apparatus of claim 23, wherein the apparatus further comprises an element that is powered by the power supply voltage and that is driven by the clock signal.

25. The apparatus of claim 17, wherein the frequency control circuit comprises a device to issue a code representing a desired voltage.

26. The apparatus of claim 25, wherein the power supply voltage is provided by the voltage regulator based on the code.

27. The apparatus of claim 17, wherein the frequency control circuit comprises a device to receive a first clock signal and a second clock signal and to output at least a signal indicative of a desired voltage level based on the first clock signal and the second clock signal.

28. The apparatus of claim 27, wherein the device is provided within a core of an integrated circuit, and the first clock signal comprises a system clock produced external from the core.

29. The apparatus of claim 17, further comprising a software selectable switch to select between at least a frequency maximizing mode and a power minimizing mode.

30. The apparatus of claim 17, wherein said frequency control circuit selects among a plurality of speed targets.

31. An apparatus comprising:

a processor core having a frequency control circuit and a first circuit to operate at a frequency dependent on a power supply voltage; and

a power source located external to the core to provide the power supply voltage to power the first circuit based on a signal received from the processor core, the frequency control circuit to control the frequency of the circuit by adjusting a level of the power supply voltage provided to the first circuit.

32. The apparatus of claim 31, wherein the frequency control circuit controls the frequency of the first circuit by directing a power source to one of increase and decrease the power supply voltage.

33. The apparatus of claim 31, wherein the frequency control circuit includes a second circuit to sense the frequency of the first circuit.

34. The apparatus of claim 31, wherein the frequency control circuit includes a second circuit to sense a temperature about said first circuit.

35. The apparatus of claim 31, wherein the first circuit provides a clock signal.

36. The apparatus of claim 35, wherein said processor core further comprises an element that is powered by the power supply voltage and that is driven by a clock signal output from said first circuit.

37. A method comprising:

operating a circuit at a frequency that is dependent on a power supply voltage; and

controlling the frequency of the circuit.

38. The method of claim 37, wherein the frequency is controlled by directing a voltage regulator to one of increase and decrease the power supply voltage.

39. The method of claim 37, further comprising powering an element by the power supply voltage and driving the element with a signal from the circuit.

40. The method of claim 37, wherein controlling the frequency comprises issuing a code representing a desired voltage.

41. The method of claim 40, wherein the power supply voltage is provided by a power source based on the code.

42. The method of claim 37, wherein controlling the frequency comprises a receiving a first clock signal and a second clock signal and outputting at least a signal indicative of a desired voltage level based on the first clock signal and the second clock signal.

43. The method of claim 42, wherein the device is provided within a core of an integrated circuit.

44. The method of claim 43, wherein the first clock signal comprises a system clock produced external from the core.

45. The method of claim 37, wherein operating the circuit comprises producing clock signals by a plurality of distributed oscillators.

46. The method of claim 45, wherein controlling the frequency comprises adjusting a level of the power supply voltage that powers the plurality of distributed oscillators.

47. A mechanism comprising:

a component to output a signal at a frequency dependent on a power supply voltage; and

a device to control a frequency of the signal by adjusting the power supply voltage.

48. The mechanism of claim 47, further comprising an element to receive the signal from a clock distribution network coupled to the component.

49. The mechanism of claim 48, wherein the power supply voltage powers the element.

50. The mechanism of claim 47, wherein the device to receive a first clock signal and a second clock signal and to output at least a signal indicative of a desired voltage level based on the first clock signal and the second clock signal.

51. The mechanism of claim 50, wherein the device is provided within a core of an integrated circuit, and the first clock signal comprises a system clock produced external from the core.

52. A mechanism comprising:

a component to output a signal at a frequency dependent on a power supply voltage; and

means for controlling a frequency of the signal by adjusting the power supply voltage.

53. The mechanism of claim 52, further comprising an element to receive the signal from a clock distribution network coupled to the component.

54. The mechanism of claim 53, wherein the power supply voltage powers the element.

55. The mechanism of claim 52, wherein the means for adjusting receives a first clock signal and a second clock signal and outputs at least a signal indicative of a desired voltage level based on the first clock signal and the second clock signal.

56. The mechanism of claim 55, wherein the means for controlling is provided within a core of an integrated circuit, and the first clock signal comprises a system clock produced external from the core.

57. A processor core comprising:

a component to produce a signal at a frequency dependent on a power supply voltage; and

a device to adjust the frequency by producing signals indicative of a desired power supply voltage to power the component.

58. The processor core of claim 57, further comprising an element to receive the signal from a clock distribution network coupled to the component.

59. The processor core of claim 58, wherein the power supply voltage powers the element.